Notice of Allowability	Application No.	Applicant(s)	
	10/603,217	EDWARDS, ERIC E.	
	Examiner	Art Unit	
	Terry L. Englund	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amdt (Sep 30, 2005) and RCE (Oct 27, 2005)*.

2. ☒ The allowed claim(s) is/are *2-4, 7, 9-13, and 19-20 (now renumbered as 2-3, 1, 4, 6-8, 5, and 9-11, respectively for printing purposes)*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *11072005* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to the applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the applicant's representative Kim Kanzaki (Reg. No. 37,652) on Nov 7, 2005.

The application has been amended as follows:

Claim 2, lines 1-2: changed "at least one" to --first--;

Claim 4, line 7: added the phrase --a second resistor coupled in parallel with the feedback transistor;-- after "transistor;";

Claim 6: cancelled in its entirety;

Claim 7, line 1: changed "claim 6" to --claim 4--; and

line 2: changed "resistor" to --resistors--.

Since the applicant had amended independent claim 4 to recite "a first diode connected transistor coupled between the first input...", dependent claim 2 was changed to more clearly refer back to that single transistor. Claim 4 was amended, by adding the basic limitation of claim 6 (now cancelled), to clearly read over Fig. 7 of Kwon's reference, as discussed with the applicant's representative, and described later. The dependency of claim 7 had to be changed since claim 6 has now been cancelled, and an inadvertent oversight on line 2 of claim 7 was also addressed (i.e. the singular "resistor" did not correspond to its preceding "first and second" phrase, and this oversight was not identified in a previous Office Action).

RESPONSE TO AMENDMENT/RCE

The amendment submitted on Sep 30, 2005, and the RCE submitted on Oct 27, 2005, have been reviewed and considered with the following results:

The RCE was approved and entered. Therefore, the amendment was also entered for consideration.

Amended claims 10 and 20 overcame their objections described in the previous Office Action. Therefore, those objections have now been withdrawn.

The cancellation of claims 22-23 rendered their respective rejection moot.

The applicant's amended claims overcame the rejections of: 1) claims 2-4 under 35 U.S.C. 103(a), with respect to Frisch et al./Payne et al., and also with respect to Guritz/Payne et al.; 2) claims 6-7 under 35 U.S.C. 103(a), with respect to Frisch et al./Payne et al./Degoirat et al., and also with respect to Guritz/Payne et al./Degoirat et al.; and 3) claims 9-12 under 35 U.S.C. 103(a), with respect to Guritz/Furuchi, and also with respect to Frisch et al./Furuchi. None of these references clearly shows or discloses the reset signal being coupled to the feedback transistor, or the first transistor, as now recited within independent claims 4 and 12, respectively. Therefore, all the above prior art rejections (described in the previous Office Action) have now been withdrawn.

However, after reviewing/reconsidering the various prior art references cited in previous Office Actions, and after performing an update search, it was noted that elements shown within Fig. 7 of Kwon (i.e. reference E, US 2004/00326514 A1, of the PTO-892 dated 07272004) would read on the claimed limitations of at least claims 2-4. For example, elements 300/400, inputs VS1/VS2, output /POR, transistor 103, voltage VCC, resistor 104 (and/or 105), transistor

203, transistor 205, and signal /POR would correspond to the claimed comparator, first/second inputs, output, first diode connected transistor, power supply voltage, first resistor, second diode connected transistor, feedback transistor, and reset signal, respectively recited within independent claim 4. After discussing these similarities with the applicant's representative, it was decided the basic limitation recited within claim 6 would be added into claim 4. Therefore, the Examiner's Amendment described above overcame that prior art type rejection with respect to the Kwon reference and claim 4.

Although several other concerns were noted within the claims when they were carefully reviewed and considered, these were also addressed/corrected by the Examiner's Amendment described above.

Therefore, there is no known objection or rejection remaining within the present application.

REASONS FOR ALLOWANCE

The following is an examiner's statement of reasons for allowance:

None of the prior art references reviewed and considered shows or discloses the power up reset circuit, or integrated circuit having a power up reset circuit, as recited within independent claims 4, 12, and 13. More specifically, although various references do show a reset type circuit comprising at least a comparator, two diode connected transistors, two resistors, and a switching (or feedback) type transistor, none of the references clearly shows or discloses: 1) the feedback transistor coupled to the second diode connected transistor, and also coupled in parallel with a second resistor, as now recited within claim 4, upon which claims 2-3, and 7 depend; 2) the first transistor coupled to the first diode connected transistor, the second diode connected transistor

being coupled directly to the power supply, and first/second capacitors connected between the power supply and ground, wherein the reset signal/output node is at the common connection of those capacitors, as understood from the limitations recited within claim 12, upon which claims 9-11 depend; or 3) the hysteresis circuit comprises a feedback transistor connected in parallel with a third resistor, wherein the third resistor is connected to the first diode connected transistor, as recited within claim 13, upon which claims 19-20 depend. Since there is no strong motivation to modify or combine any prior art reference(s) to ensure all of the claimed limitations within any one of the three independent claims are met, the claims are deemed patentably distinct over the prior art of record.

Claims 2-4, 7, 9-13, and 19-20 are allowed, and have been renumbered as 2-3, 1, 4, 6-8, 5, and 9-11, respectively for printing purposes. The renumbering takes into account the cancellation of claims 1, 5-6, 8, 14-18, and 21-23, as well as ensuring each independent claim is renumbered lower than its respective dependent claims.

PRIOR ART

The prior art references on the accompanying PTO-892 are cited for interest and documentation purposes only. These references were found and considered during the update search. Fig. 1 of Adams et al. closely corresponds to the basic elements (e.g. comparator, diode connected transistors, resistors, and feedback transistor) shown within the applicant's own Fig. 9. However, the reference is not valid for any prior art rejections for two main reasons: 1) It was filed on Mar 29, 2004, which is after the Jun 24, 2003 filing date of the present application; and 2) transistor MN1 and resistor R3 are shown coupled between resistor R2 and ground, wherein the present application's claimed limitations (e.g. feedback transistor, first transistor, or

hysteresis circuit with feedback transistor and third resistor) would be understood as having them coupled between MN0 and ground. Similar to the coupling explanation described above, even if transistors 48 and 50 of Phillips et al.'s Fig. 3 are considered one type of comparator (e.g. the common connection of the base of transistor 48 and the base/collector of diode connected transistor 34 would correspond to one input of the comparator, and the common connection of the base of transistor 50 and the base/collector of diode connected transistor 46 would correspond to the other input of the comparator), the feedback (first) transistor 40, along with its parallel resistor 42, would have to be coupled between diode connected transistor 46 and ground to meet the limitations recited within any one of the present application's independent claims. Since these two references clearly show and disclose the feedback/first transistor, and parallel resistor, coupled between ground and a corresponding resistor within one current path within the circuit, there is no strong motivation to insert the feedback/first transistor, and its parallel resistor, between a diode connected transistor (within the other current path) and ground.

Any comments considered necessary by the applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

7 November 2005

Kenneth B. Wells
Primary Examiner